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**Question Paper Code : 11217**

**B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016**

**Sixth Semester**

**Electrical and Electronics Engineering**

**EC 1354 – VLSI DESIGN**

**(Common to Electronics and Communication Engineering)**

**(Regulations 2008)**

**Time : Three Hours** **Maximum : 100 Marks**

**Answer ALL questions.**

**PART – A (10 × 2 = 20 Marks)**

1. Define threshold voltage of a MOS transistor.
2. Why are nMOS devices preferred over pMOS devices ?
3. How propagation delay is calculated in sequential logic circuits ?
4. Give the advantages of dynamic logic gates.
5. What do you mean by super buffer ?
6. What is stick diagram ?
7. What is cross talk ?
8. Define propagation delay.
9. Define FSM.
10. What are gate primitives ?

## PART – B (5 × 16 = 80 marks)

11. (a) Draw the small signal model of a MOS transistor and explain its AC characteristics.

**OR**

(b) (i) Explain the second order effects in MOS device design. **(8)**

(ii) Explain in detail, n well CMOS fabrication process with necessary diagrams. **(8)**

12. (a) (i) Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics. **(12)**

(ii) Explain the $\beta_n/\beta_p$ ratio. **(4)**

**OR**

(b) (i) Derive the $V_{OH}$ and $V_{OL}$ for saturated load inverter using an NMOS transistor load. **(8)**

(ii) Explain the statement "The CMOS Inverter as an Amplifier". **(8)**

13. (a) Write a technical note on the following :

(i) Power dissipation and Transistor sizing **(6)**

(ii) MOS scaling issues and alternate methods for overcoming scaling issues. **(10)**

**OR**

(b) (i) Discuss in detail the various electrical characteristics of CMOS system. **(6)**

(ii) State the importance of parameter extraction and briefly explain the different passive elements estimation methods. **(10)**

14. (a) (i) Draw the circuits for $P_i$ and $G_i$ needed for a 4 bit Carry look ahead adder in each of the following CMOS technologies:

(1) Static CMOS; (2) Domino CMOS and (3) TG logic. **(10)**

(ii) Construct a 2 × 2 array multiplier circuit with latching inputs. Write a Verilog description for the above circuit. **(6)**

**OR**

(b) Consider the 4 – bit shift register shown in Figure. 1. The data stream D consists of sequential bits d0, d1, d2, and d3. The timing is set such that the first bit d0 enters stage 0 on the first clock edge. On the next rising edge, dl enters stage 0, while d0 moves to stage 1, and so on.

(i) Write a Verilog description of the shift register using DFF modules as primitives.

(ii) Select a CMOS design techniques for the DFFs and use it to construct the circuit.

(iii) Now write a verilog description of the shift registers using nMOS and pMOS primitives.

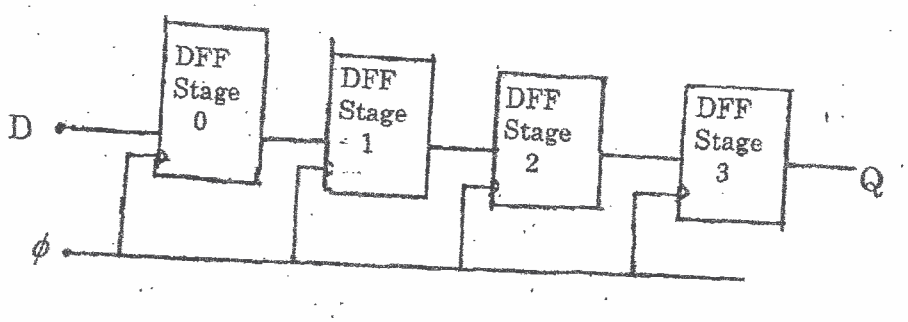


**Figure 1**

15. (a) Explain the following with an example :

(i) Tasks and functions **(4)**

(ii) Test bench for 4 : 1 multiplexer **(4)**

(iii) Difference between always and initial . **(4)**

(iv) Blocking and non-blocking statements. **(4)**

**OR**

(b) (i) Design and develop a project in HDL to compare x5x4x3x2xlx0 with y5y4y3y2yly0. Check the output by means of test bench. **(10)**

(ii) Give the different types of operators in Verilog HDL and explain any three. **(6)**

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